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09/599,005	06/22/2000	Masahiro Kaminaga	520.38691X00	8576

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EXAMINER	
ZAND, KAMBIZ	
ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,005	KAMINAGA ET AL.	
	Examiner	Art Unit	
	Kambiz Zand	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-35* is/are pending in the application.

4a) Of the above claim(s) *23-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Kambiz Zand

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35,U.S.Code not included in this section can be found in the prior office action.
2. The prior office actions are incorporated herein by reference. In particular, the observations with respect to claim language, and response to previously presented arguments.
3. Claims 1-22 have been cancelled.
4. In the light of cancellation of claims 1-22, **the status of claims 23-25 not clear** (Examiner **request clarification** if the original claims 23 (non-elected invention IV) and 24-25 (non-elected invention I) are either withdrawn or cancelled, since response to restriction (paper number 6) and response filed on 12/08/2004 are not specific.
5. **New claims 23-32**, now, re-numbered as claims 26-35 have been added (**see specification objection below**).
6. Claims 26-35 are pending.
7. Examiner withdraws objections to the originally filed declaration due to clarification by the Applicant.
8. Examiner withdraws objection to the drawings and specification due to correction by the Applicant and Applicant's arguments filed on 12/08/2004.
9. Examiner withdraws rejection of claims 7,8,10,11 and 21-22 under 35 U.S.C 112-second paragraphs due to cancellation of the claims by the Applicant.

Information Disclosure Statement PTO-1449

10. The Information Disclosure Statement submitted by applicant on 07/28/2004 has been considered. Please see attached PTO-1449.

Specification

11. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered new claims 23-32 have been renumbered as claims 26-35.

Claim Objections

12. **Claims 31 and 33-35** are objected to because of the following informalities: typo error. Examiner suggests the following corrections:

Claim 31

- Replacement of the phrase "the" (first occurrence, line 3) with the phrase - -a- -.
- Replacement of the phrase "the" (second occurrence, line 6) with the phrase - - a- -.

Claim 33:

- Replacement of the phrase "decryption" (line 8) with the phrase "encryption".

13. **Claims 34-35** are objected to as being dependent on the objected claim 33.

Response to Arguments

15. Applicant's arguments filed 12/08/2004 with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

16. **Claims 26-30 and 33-35** are rejected under 35 U.S.C. 102(b) as being anticipated by Morris et al (4,503,287).

17. **As per claim 26** by Morris et al (4,503,287) teach a semiconductor chip in which information of two values corresponds to two different voltage comprising:

information such as generation of keys or encryption/decryption process of information; or other process by terminal 16 and host 12 including transmission of data which is an information process; abstract);

An information memory device (see items 34, 35, 38, 39, 40 and 41 where examiner considers any storage device and/ or a memory within terminal 16 and 12 corresponding to Applicant's memory device);

An encryption device (see fig.2, items 42 or 43 where examiner considers cipher device as corresponding to encryption device);

A decryption device (see fig.2, items 42, 43 where examiner considers decipher device corresponding to Applicant's decryption device); and a data bus (see any links between item 42, 43 or other blocks to each other as having inherent data bus; The reasons for inherency is that any transfer of data to or from a processing unit or storage device uses a bus for the communication that is called data bus (see IEEE standard dictionary, seven edition); abstract disclose transfer of data and storage of it; fig.2 disclose the links and col.3, lines 28-59 discloses such transfer of data to and from the above information processing units and storages devices),

Wherein data is transferred from the information processing device to the information memory device through the data bus and stored in the information memory device after the data has been encrypted by the encryption device, and wherein data read from the information memory device is input into the information processing device through the data bus after the data has been

decrypted by the decryption device (see col.4, lines 28-67; col.4, lines 1-5 and in harmony with all above definition given by examiner).

- The recitation "a semiconductor chip in which information of two values corresponds to two different voltage" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

As per claim 27 Morris et al (4,503,287) teach the semiconductor chip according to claim 26, wherein the encryption performed by the encryption device is an exclusive OR operation of the data output from the information processing device and key data, and wherein the decryption performed by the decryption device is exclusively OR operation by the data read from the information memory device and a key data (see col.4, lines 7-16 where it uses DES algorithm; exclusive operation is inherent part of DES algorithm by standard; please see definition of DES algorithm in any crypto dictionary).

As per claims 28 Morris et al (4,503,287) teach the semiconductor chip according to claims 26, wherein the encryption performed by the encryption device is an exclusive OR operation of the data output from the information processing device and key data appended to part of destination address data of the data in the information memory device; and

Wherein the decryption performed by the decryption device is an exclusive OR operation of the data read from the information memory device and key data appended to a part of source address data of the data in the information memory device (see col.4, lines 7-16 where it uses DES algorithm; exclusive operation is inherent part of DES algorithm by standard; please see definition of DES algorithm in any crypto dictionary and fig.2 and associated text).

As per claims 29 and 35 Morris et al (4,503,287) teach the semiconductor chip according to claim 27, 34 further comprising: a random number generator, wherein the key data is a random number generated by the random number generator (see col.3, lines 41-43).

As per claim 30 Morris et al (4,503,287) teach the semiconductor chip according to claims 27, further comprising:

A key buffer which is writable from the information processing device, wherein the key buffer stores the key data transferred from the information processing device (see fig.4 and 5 and associated text; col.5, lines 34-52).

As per claim 32 Morris et al (4,503,287) teach the semiconductor chip according to claim 26, wherein the encryption device determines whether to encrypt the data output from the information processing device according to the data pattern; and

Wherein the decryption device determines whether to decrypt the data read from the information memory device unit according to the data pattern (see col.5, lines 34-52 with special attention to lines 43-46 where the most significant bit determines the data pattern and if the enciphering is needed).

As per claim 33 Morris et al (4,503,287) teach a semiconductor chip in which information of two values corresponds to two different voltage comprising:

An information processing device (see fig.2, item 16, 12, 36, 37, 42 and 43 and their associated text, where all the items mentioned are capable of processing information such as generation of keys or encryption/decryption process of information; or other process by terminal 16 and host 12 including transmission of data which is an information process; abstract);

An information memory device (see items 34, 35, 38, 39, 40 and 41 where examiner considers any storage device and/ or a memory within terminal 16 and 12 corresponding to Applicant's memory device);

A first encryption device (see fig.2, items 42 where examiner considers cipher device 42 as corresponding to first encryption device);

A second decryption device (see fig.2, items 43 where examiner considers decipher device as corresponding to second decryption device);

A first decryption device (see fig.2, items 42 where examiner considers decipher device as corresponding to first decryption device);

A second encryption device (see fig.2, items 43 where examiner considers encipher device as corresponding to second encryption device); and a data bus (see any links between item 42, 43 or other blocks to each other as having inherent data bus; The reasons for inherency is that any transfer of data to or from a processing unit or storage device uses a bus for the communication that is called data bus (see IEEE standard dictionary, seven edition); abstract disclose transfer of data and storage of it; fig.2 disclose the links and col.3, lines 28-59 discloses such transfer of data to and from the above information processing units and storages devices),

Wherein data output from the information processing device is encrypted by the first encryption device and output to the data bus, wherein the data encrypted by the first encryption device is transferred to the first decryption device through the data bus, decrypted by the first decryption device and stored in the memory device, wherein the data read from the information memory device is encrypted by the second encryption device and output to the data bus, and wherein the data encrypted by the second encryption device is transferred to the second decryption device through the data bus, decrypted by the second decryption device and input to the information processing device (see fig.2 and associated text where the encryption decryption process is of data is between item 42 and 43 and vice versa, reading from storage devices 40 and 41 in unidirectional process as has been described in the above limitation).

- The recitation "a semiconductor chip in which information of two values corresponds to two different voltage" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

As per claim 34 Morris et al (4,503,287) teach the semiconductor chip according to claim 33, wherein the encryption performed by the first encryption device is an exclusive OR operation of the data output from the information processing device and key data, wherein the encryption performed by the second encryption device is an exclusive OR operation of the data transferred from the first encryption device and the key data, and wherein the decryption performed by the second decryption device is an exclusive operation of the data transferred from the second encryption device and the key data (see col.4, lines 7-16 where it uses DES algorithm; exclusive operation is inherent part of DES algorithm by standard; please see definition of DES algorithm in any crypto dictionary and fig.2 and associated text).

Examiner suggests the attention to the page 4-6 of Applicant's specification where the heart of the invention is described and the above claims limitations are not represented those factors.

Claim Rejections - 35 USC § 103

18. **Claim 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al (4,503,287) in view of Rothenberg (5,432,850 A).

As per claim 31 Morris et al (4,503,287) teach all limitation of the claims but do not explicitly disclose, wherein the encryption device determines whether to encrypt the data output from the information processing device according to the destination address of the data in the information memory device; and Wherein the decryption device determines whether to decrypt the data read from the information memory device according to the source address of the data in the information memory device.

However Rothenberg (5,432,850 A) disclose the encryption device determines whether to encrypt the data output from the information processing device according to the destination address of the data in the information memory device; and Wherein the decryption device determines whether to decrypt the data read from the information memory device according to the source address of the data in the information memory device (see abstract; fig.2a,2b and 4 and associated text). It

would have been obvious to one of ordinary skilled in the art at the time the invention was made to utilize Rothenberg's source and destination address in Morris's buffer using Morris's most significant bit of the address to enable encryption or decryption based on the address in the buffer in order to have means for employing the local address of the receiver or sender for encryption and decryption (see col.2, lines 36-54)

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kambiz Zand whose telephone number is (571) 272-3811. The examiner can normally reached on Monday-Thursday (8:00-5:00). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone numbers for the organization where this application or proceeding is assigned as (703) 872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kambiz Zand

05/11/2005

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FIG.1 Prior art

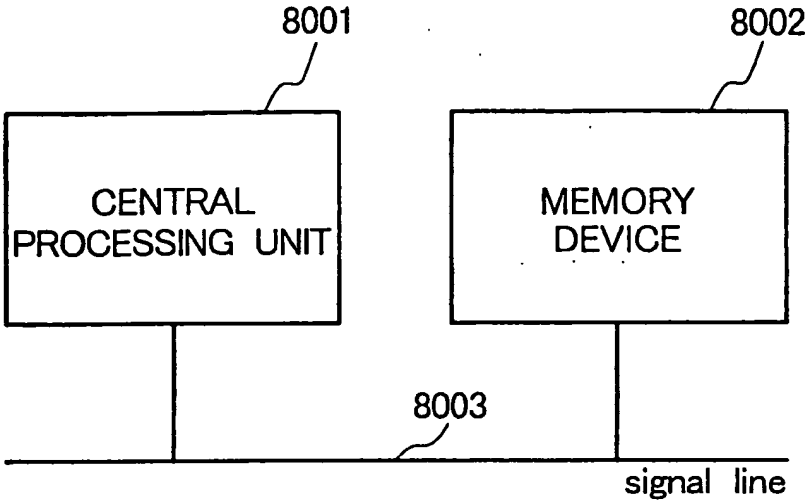

FIG.2 Prior art

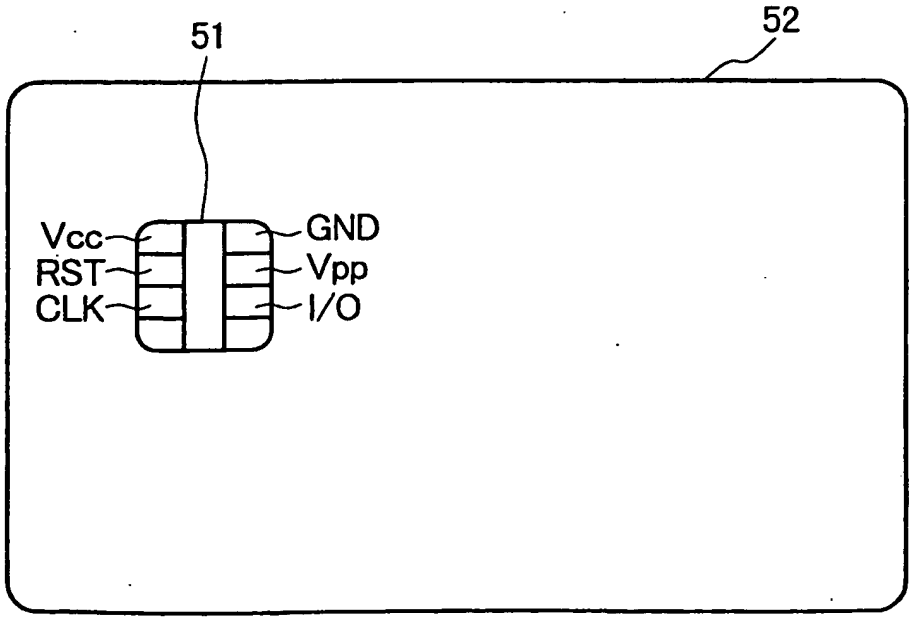

FIG.3

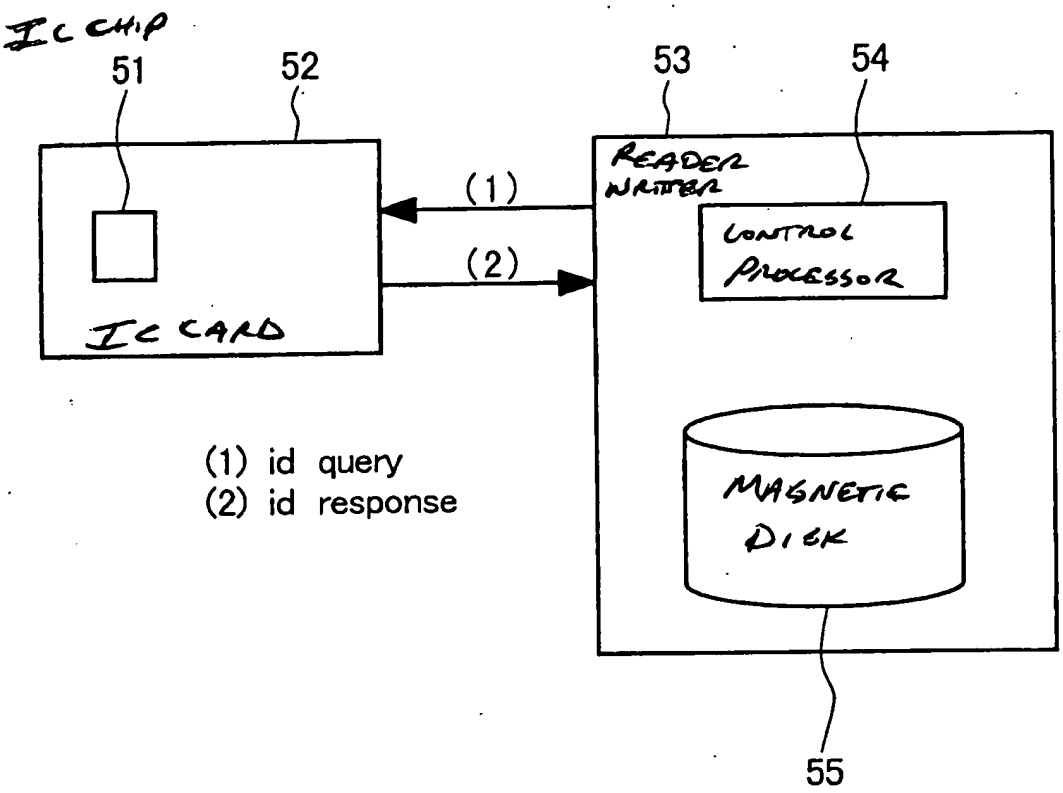

FIG.4